

WHAT IS CLAIMED IS:

1. A variable resolution analog-to-digital converter comprising:

5 a sample-and-hold circuit including a plurality of sample-and-hold units which are connected in parallel and selectively activated corresponding to a required resolution to sample and hold an analog input signal;

10 a plurality of conversion stages connected in cascade to an output of the sample-and-hold circuit to convert an output signal of the sample-and-hold circuit to a plurality of bit signals; and

a synthesis circuit to synthesize the bit signals to generate a digital output signal.

15 2. The variable resolution analog-to-digital converter according to claim 1, wherein the conversion stages comprise a plurality of variable conversion stages in cascade to the output of the sample-and-hold circuit and a plurality of non-variable conversion stages in cascade to a last one of the variable
20 conversion stages, each of the variable conversion stages including a first sub-analog-to-digital converter unit configured to convert a first analog signal to a first digital signal and a plurality of first sub-multiplying-digital-to-analog converter units
25 connected in parallel and selectively used according to the required resolution to convert the first digital signal to a second analog signal, generate a first

difference signal between the first analog signal and the second analog signal and multiply the first difference signal by a give value, the first analog signal being an analog signal corresponding to the analog input signal.

3. A variable resolution analog-to-digital converter comprising:

a sample-and-hold circuit including a plurality of sample-and-hold units connected in parallel and selectively activated corresponding to a required resolution to sample and hold an analog input signal;

a plurality of first conversion stages connected in cascade to an output of the sample-and-hold circuit, each of the first conversion stages including a first sub-analog-to-digital converter unit configured to convert a first analog signal to a first digital signal and a plurality of first sub-multiplying-digital-to-analog converter units connected in parallel and selectively activated according to the required resolution to convert the first digital signal to a second analog signal, generate a first difference signal between the first analog signal and the second analog signal and multiply the first difference signal by a given value, the first analog signal being an analog signal corresponding to the analog input signal;

a plurality of second conversion stages connected

in cascade to an output of a last one of the first conversion stages, each of the second conversion stages including a second sub-analog-to-digital converter unit configured to convert a third analog signal into
5 a second digital signal and a second sub-digital-to-analog converter unit to convert the second digital signal into a fourth analog signal and output a second difference signal between the third analog signal and the fourth analog signal, the third analog signal being
10 an analog signal corresponding to the analog input signal; and

a synthesis circuit to synthesize the first digital signal output from each of the first conversion stages and the second digital signal output from each
15 of the second conversion stages, to generate a digital output signal.

4. The variable resolution analog-to-digital converter according to claim 3, wherein the first conversion stages each include a switch unit to connect
20 all of the sample-and-hold units in parallel when the required resolution is a first resolution and to connect one of the sample-and-hold units when it is a second resolution lower than the first resolution.

5. The variable resolution analog-to-digital converter according to claim 3, wherein the first
25 conversion stages each include a switch unit to connect all of the sub-digital-to-analog converter

units in parallel when the required resolution is a first resolution and to connect one of the sub-digital-to-analog converter units when it is a second resolution lower than the first resolution.

5 6. The variable resolution analog-to-digital converter according to claim 3, which includes a third sub-analog-to-digital connected to a last one of the second conversion stages to convert the a second difference signal output from the last one of the
10 second conversion stages into a digital signal.

 7. The variable resolution analog-to-digital converter according to claim 3, wherein the first conversion stages are used for most significant bits and the second conversion stages are used for least
15 significant bits.

 8. The variable resolution analog-to-digital converter according to claim 3, wherein an initial one of the first conversion stages is supplied with an output signal of the sample-and-hold circuit as the
20 first analog signal, and each of the remaining ones of the first conversion stages is supplied, as the first analog signal, with the first difference signal of a preceding one of the first conversion stages that is multiplied by the given value.

25 9. The variable resolution analog-to-digital converter according to claim 3, wherein an initial one of the second conversion stages is supplied with

the first difference signal of a last one of the first conversion stages as the third analog signal, and each of the remaining ones of the second conversion stages is supplied with the second difference signal of
5 a preceding one of the second conversion stages as the third analog signal.

10. The variable resolution analog-to-digital converter according to claim 3, wherein the second sub-digital-to-analog converter unit includes
10 a digital-to-analog converter unit to convert the second digital signal into the fourth analog signal, a subtracter to subtract the fourth analog signal from the third analog signal to output the second difference signal, and a residual amplifier to amplify the second
15 difference signal.

11. A variable resolution analog-to-digital converter comprising:

a sample-and-hold circuit including a plurality of sample-and-hold units which are connected in parallel
20 and selectively used corresponding to a required resolution to sample and hold an analog input signal;

a plurality of conversion stages connected in cascade to an output of the sample-and-hold circuit, each of the conversion stages including a sub-analog-to-digital converter unit configured to convert a first
25 analog signal into a digital signal and a sub-digital-to-analog converter unit to convert the digital signal

into a second analog signal and output a difference signal between the first analog signal and the second analog signal, the first analog signal being an analog signal corresponding to the analog input signal; and

5 a switch which turns on or off according to the required resolution to bypass at least an initial stage of the conversion stages; and

 a synthesis circuit configured to synthesize digital signals each provided by each of the conversion stages, to generate a digital output signal.

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12. The variable resolution analog-to-digital converter according to claim 11, which further includes a clock phase inverting circuit configured to inverse, when the switch turns on, a phase of a clock signal supplied to the conversion stages except for at least the initial one of the conversion stages with respect to a phase of the clock signal when the switch turns off.

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13. A variable resolution analog-to-digital converter comprising:

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 a sample-and-hold circuit including a plurality of sample-and-hold units which are connected in parallel and selectively used according to a required resolution to sample and hold an analog input signal;

25 a plurality of unit delay circuits connected in cascade to delay an output signal from the sample-and-hold circuit;

an analog linear transformation circuit to subject a set of output signals from the unit delay circuits to a first linear transformation to output a plurality of linear transformed analog signal;

5 a plurality of sub-analog-to-digital converter units to convert the linear transformed analog signal into a plurality of digital signals;

 a digital linear transformation circuit to subject a set of digital signals of the digital signals output
10 from the sub-analog-to-digital converter units to a second linear conversion that is an inverting transformation of the first linear transform, to output a plurality of digital signals output by the sub-analog-to-digitals; and

15 a digital delay adder circuit to add the linear digital signals with the same delay time as that of the analog delay circuit to generate a digital output signal.

 14. The variable resolution analog-to-digital
20 converter according to claim 13, wherein each of the unit delay circuits include a plurality of sub-delay circuits connected in parallel selectively according to the required resolution to delay an output signal from the sample-and-hold circuit.

25 15. The variable resolution analog-to-digital converter according to claim 13, wherein the analog linear transformation circuit comprises a variable

analog linear transformation circuit whose linear transformation matrix is variable and the sub-analog-to-digital converter units are selectively used according to at least one signal from the variable analog linear transformation circuit, the number of used sub-analog-to-digital converter units being determined by the required resolution.

16. The variable resolution analog-to-digital converter according to claim 15, wherein the digital linear transformation circuit comprises a variable digital linear transformation circuit whose linear transformation matrix is variable.

17. A radio receiver comprising:
a high frequency filter to filter a receive signal;
a low noise amplifier circuit to amplify the filtered receive signal;
a frequency converter to convert the filtered receive signal into an intermediate frequency signal;
an intermediate filter to filter the intermediate frequency signal;
a variable gain amplifier to amplify the filtered intermediate frequency signal;
a frequency converter to convert the amplified intermediate frequency signal into a low frequency signal; and
the variable resolution analog-to-digital circuit

according to claim 3 to subject the low frequency signal to a variable resolution analog-to-digital conversion.